THE FIELD GUIDE

The Investors Guide to Semiconductors

Six business models hide under one label. This is the one-page-per-model field guide to telling them apart — what each one actually does, the single number that tells you if it's working, and the single red flag that breaks it.

97.5%

ARM GROSS MARGIN
ROYALTY MACHINE

→ • • • →

-9.1%

MICRON TROUGH MARGIN
COMMODITY CYCLICAL

Same “sector.” A 106-point gap in gross margin. There is no such thing as *a* semiconductor stock.

00

HOW TO READ THIS

One map. Two axes. Six business models.

The value chain

IDEA → FINISHED CHIP

01	02	03	04	05	06
IP	→ EDA	→ Fabless	→ Manufacturer	→ Memory	→ Equipment

The map

TWO AXES, SIX MODELS

Every company sits on two axes: gross margin (Y — how good the underlying model is) against capital intensity, capex ÷ revenue (X — how much cash it burns just to compete). Walk the chain and the pin moves: asset-light at the top, a plunge into the capital-heavy manufacturing and memory pit, then a climb back out to the equipment monopolies.

WHY GROSS MARGIN, NOT P/E

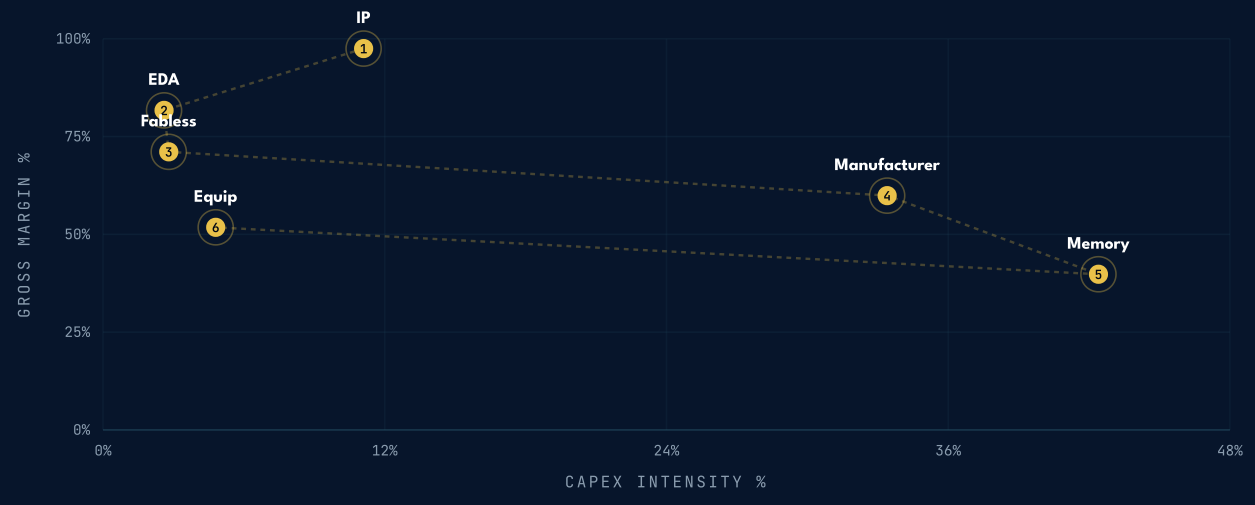
Gross margin isolates the structural economics of the model. Operating margin buries it under opex choices; EBITDA flatters the capital-heavy names; P/E is actively misleading on a cyclical. Start with the business, not the multiple.

BUT HIGHER ISN'T BETTER

A high gross margin is **not** a buy signal. It tells you what **kind** of business you own — not whether the stock is cheap. ARM keeps 97.5¢ on the dollar and still hands most of it back in R&D, so its operating margin is just 18%. The map gives you the model; never the verdict.

THE MARGIN MAP · ALL SIX BUCKETS

Y = GROSS MARGIN · X = CAPEX INTENSITY



Y · MARGIN

Gross margin, most recent full fiscal year. The higher the pin, the better the raw economics of the business model.

X · CAPITAL

Capex ÷ revenue. The further right, the more cash sunk into plant just to compete. SMIC runs ~90% — off-chart.

READ IT

Durable wealth clusters at the extremes — asset-light top-left and monopoly equipment — not the crowded, capital-hungry middle.

01

VALUE CHAIN · THE BLUEPRINT

The Royalty Machines

License the chip's architecture, collect a royalty on every unit ever built on it. No factory, no wafer, no inventory — the purest asset-light model in the industry.

ARM — pure-play | CEVA | (Qualcomm QTL — see 03)

GROSS MARGIN	OP MARGIN	ROIC	CAPEX	R&D INTENSITY
87–97.5%	18%	15–25%	1–11%	60–70%

ARM is the pure-play benchmark (GM 97.5%, op margin 18.3%). **CEVA op margin −10.4%** — a sub-scale outlier. ARM capex is now 11.1%, up from near-zero, on its AI/compute buildout.

THE METRIC TO WATCH

Royalty rate per chip

Value captured per unit — it climbs as customers adopt newer architectures (the v8 → v9 shift). Also track the licensing-vs-royalty mix: licensing leads, royalties lag.

THE RED FLAG

The R&D trap

Must fund next-gen architecture years before royalties arrive. A design-cycle lull flattens revenue while opex keeps compounding — the risk moved from the factory floor to the R&D lab.

ALSO WORTH WATCHING

+ License backlog / pipeline (Total Access + Flexible Access counts)
+ Licensing-to-royalty revenue mix as a leading indicator
+ The GAAP / non-GAAP gap — SBC and R&D compress GAAP hard

OTHER RISKS

– Customer concentration among a few large licensees
– Royalty rate stagnating while unit volumes rise
– RISC-V displacement — real in embedded, overstated in high-performance compute

> **"Watch the royalty per chip. The trap: they spend for tomorrow's chips today — if the design cycle stalls, margins bleed while the R&D bill keeps climbing."**

02

VALUE CHAIN · THE DESIGN SOFTWARE

The Software Toll Booth

The software every advanced chip is designed in. A near-duopoly protected by years-deep switching costs and foundry co-optimization — you don't rip these tools out.

Synopsys | Cadence | Siemens EDA — buried in Siemens

GROSS MARGIN	OP MARGIN	ROIC	CAPEX	R&D INTENSITY
77–86%	13–28%	3–18% incl. goodwill	<4%	30–36%

Cadence is the clean end (GM 86.4%, op margin 28.2%). **Synopsys ROIC ~3%** and op margin 13% reflect the $26.9B Ansys goodwill dragging returns — hence the wide spread.

THE METRIC TO WATCH

RPO / backlog

Remaining Performance Obligations — contracted revenue not yet booked. A leading indicator of customer commitment; Cadence closed FY25 at a record ~$7.8B. Demand tracks customers' R&D budgets, not wafer volumes.

THE RED FLAG

Growth bought, not built

A mature duopoly has to acquire to grow fast. Decompose organic vs. acquired growth. Synopsys leaned in too hard on Ansys — $26.9B goodwill now exceeds equity, tangible book –$12.4B. Cadence is the disciplined counter-example.

ALSO WORTH WATCHING

+ Customer R&D spend & design starts — the true demand driver
+ Emulation hardware cycle (Palladium / ZeBu) drives product spikes
+ Organic growth rate stripped of acquisitions

OTHER RISKS

– China revenue exposure + export-control whipsaw (~10–16% at SNPS)
– Post-deal integration & goodwill impairment risk
– Reverse DCF demanding aggressive perpetual growth, no margin of safety

> **"Watch the backlog for demand — then check whether the growth is organic or bought. Synopsys shows what leaning in too hard looks like; Cadence shows the disciplined version."**

03

VALUE CHAIN · THE DESIGNERS

The Designers Everyone Chases

Design the chip, outsource the manufacturing to a foundry. Capital-light and high-margin when product leadership holds — the bucket almost every retail portfolio already owns.

NVIDIA | Broadcom | AMD | Qualcomm — also IP (QTL) | Marvell · MediaTek | Apple — captive

GROSS MARGIN	OP MARGIN	ROIC	CAPEX	R&D INTENSITY
50–75%	10–60%	6–17%	<3%	10–20%

Spread runs wide: AMD op margin 10.7% to NVIDIA 60.4%. **NVIDIA ROIC ~175%** is a clear outlier well above the 6–17% bucket range — don't read it as typical.

THE METRIC TO WATCH

Inventory days + purchase commitments

Days Inventory Outstanding plus how much capacity they've pre-ordered from the foundry. Rising inventory paired with big non-cancelable commitments is the setup for a shock.

THE RED FLAG

Purchase-obligation shock

Non-cancelable wafer orders placed ~a year ahead on a forecast. When demand or regulation turns, they become a writedown overnight — NVIDIA's $4.5B H20 charge in Q1 FY26 is the live example.

ALSO WORTH WATCHING

+ Product cadence (NVDA's yearly Hopper → Blackwell → Rubin)
+ Gross-margin trend — pricing power vs. commoditization
+ CoWoS / advanced-packaging allocation as a hard ceiling on shipments

OTHER RISKS

– Single-product or single-customer dependence
– Margin compression signalling lost pricing power
– Valuation pricing peak-cycle margins as permanent

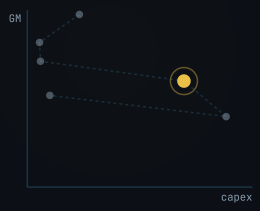
> **"Watch inventory days and what they've locked in with the foundry. Asset-light works until demand turns — then those non-cancelable orders become a writedown."**

04

VALUE CHAIN · WHO ACTUALLY BUILDS IT

The Builders

Where capital intensity explodes. Three different jobs — pure foundry, integrated design-and-make, and outsourced packaging — that share a manufacturing risk profile the design side never touches.



4a Foundry

PURE-PLAY MAKE

TSMC · UMC · GF · SMIC (capex ~90%, off-chart)

GM	21–60%	OP MGN	7–51%
ROIC	1–36%	CAPEX	11–33%
R&D	8–12%		

METRIC

Capacity utilization + advanced-node revenue share.

RED FLAG

Depreciation overwhelm — an empty new node depreciates from day one.

4b IDM

DESIGN + OWN FABS

Intel · TI · Infineon · NXP · STMicro

GM	29–57%	OP MGN	-4–34%
ROIC	0–20%	CAPEX	3–28%
R&D	12–27%		

METRIC

Distributor channel days + book-to-bill.

RED FLAG

Under-absorption — idle fabs dump fixed cost straight into COGS.

4c OSAT

PACKAGE & TEST

ASE · Amkor · JCET

GM	14–18%	OP MGN	7–8%
ROIC	4–9%	CAPEX	13–26%
R&D	4–5%		

METRIC

Advanced-packaging mix (CoWoS / SiP share).

RED FLAG

Commoditization — standard packaging is a price-taker at break-even.

THE THROUGH-LINE

Utilization is everything

All three live and die on how full the lines run. Fixed costs are enormous and sunk; below ~80% utilization, unabsorbed depreciation and overhead crush margins fast. This is operating leverage in reverse.

THE INSIDER COUNTER-THESIS

Asset-heavy can still win

"Asset-light always wins" is wrong when a manufacturer builds a scale monopoly. TSMC's yield-learning loop and reinvestment wall produced a ~40.5% ROE — beating many asset-light designers. Capital intensity isn't automatically a flaw.

> **"Watch utilization — a fab below ~80% full bleeds. The trap is building capacity ahead of demand: the depreciation clock starts whether the orders show up or not."**

05

VALUE CHAIN · THE CYCLICAL MONSTER

The Commodity Cyclical

DRAM and NAND are commodities — price is set by industry supply and demand, not the company. The most violently cyclical bucket on the map, and the one where the "cheap P/E" trap lives.

Samsung — SOTP | SK Hynix | Micron | Kioxia · SanDisk / WDC

−9.1% → +58.9%

Micron's gross margin across a single decade — trough to peak. SK Hynix swung from −1.6% to +62.4% over the same span. No other bucket moves like this. The same company, the same product, can lose money on every chip one year and print 60-point margins the next.

GM · PEAK → TROUGH	OP MARGIN SWING	CAPEX · PEAK	ROIC	R&D INTENSITY
62 → -9%	50 → -40%	30–45%	35 → neg	7–10%

The range is the whole point. **Micron today: GM 39.8%, op margin 26.1%** — mid-cycle, off both extremes. SK Hynix sits near the top at ~60% GM on the HBM boom.

THE METRIC TO WATCH

Spot vs. contract pricing

Spot leads contract. Pair it with inventory weeks at both producer and customer level, and HBM capex allocation — HBM eats ~3× the wafer capacity of standard DRAM, structurally tightening supply.

THE RED FLAG

The low-P/E-at-peak value trap

Peak earnings on peak pricing make the stock look cheapest right before the collapse. A single-digit trailing P/E on a memory maker usually means the top is in — you're buying peak earnings about to vanish.

> **"Watch the pricing trend, not the P/E. In memory, a single-digit trailing P/E usually means the top is in — you're buying peak earnings that are about to vanish."**

06

VALUE CHAIN · PICKS & SHOVELS

The Toolmakers

Sell the machines that build every fab, then lock customers into decades of high-margin service and spares. The twist ending: asset-light, near-monopoly economics at the bottom of the chain.

ASML — EUV monopoly | Applied Materials | Lam Research | KLA | Tokyo Electron · Advantest

GROSS MARGIN	OP MARGIN	ROIC	CAPEX	R&D INTENSITY
45–61%	26–40%	25–50%	3–9%	10–15%

THE METRIC TO WATCH

Book-to-bill + service mix

Book-to-bill above 1 signals a growing capex cycle — it's the leading indicator. The service and installed-base revenue share is the quality signal: a non-discretionary cushion that carries earnings through the down-cycle.

THE RED FLAG

The geopolitical export cliff

Leading-edge equipment is a primary geopolitical lever. A single export ban can erase 20–40% of the addressable market overnight and render backlog obsolete — the one risk you can't model in a spreadsheet.

ALSO WORTH WATCHING

+ Order backlog & lead times (12–18 months for advanced litho)
+ Aggregate customer capex guidance (TSMC / Intel / Samsung / memory)
+ Service & install-base share as a recurring-revenue cushion

OTHER RISKS

– Book-to-bill falling below 1 — the cycle rolling over
– Customer concentration — a handful of fabs is the whole market
– Peak orders extrapolated as a permanent run-rate

> **"Watch book-to-bill for the cycle and the service mix for durability. The one risk you can't model: a pen stroke in Washington that deletes a third of the market."**

ONE PAGE · PRINT IT · PIN IT

Cheatsheet

Eight rows, because manufacturing is really three different businesses. Read it top to bottom and you're walking the value chain — asset-light and high-margin at the top, capital-heavy and cyclical through the middle, back to monopoly economics at the end.

BUCKET	COMPANIES	GROSS MARGIN	CAPEX INTENSITY	THE METRIC TO WATCH	THE RED FLAG
IP Licensors 01	ARM	87–97.5%	1–11%	Royalty rate per chip; licensing-vs-royalty mix	**R&D trap** — funds tomorrow's chips today; a design lull bleeds margin
EDA 02	Synopsys, Cadence	77–86%	<4%	RPO / backlog; organic vs. acquired growth	**Growth bought, not built** — M&A masks slow organic growth (SNPS/Ansys)
Fabless 03	NVDA, AVGO, AMD, QCOM	50–75%	<3%	Inventory days + non-cancelable purchase commitments	**Obligation shock** — pre-ordered wafers become a writedown (H20 $4.5B)
Foundry 04A	TSMC, UMC, GF, SMIC	21–60%	11–33%	Capacity utilization + advanced-node share	**Depreciation overwhelm** — an empty new node depreciates from day one
IDM 04B	Intel, TI, NXP, STMicro	29–57%	3–28%	Distributor channel days + book-to-bill	**Under-absorption** — idle fabs charge fixed cost straight to COGS
OSAT 04C	ASE, Amkor	14–18%	13–26%	Advanced-packaging mix (CoWoS / SiP)	**Commoditization** — standard packaging is a price-taker at break-even
Memory 05	Micron, SK Hynix, Samsung	-9 → 62%	30–45%	Spot vs. contract pricing + inventory weeks	**Low-P/E-at-peak trap** — looks cheapest right before the collapse
Equipment 06	ASML, AMAT, Lam, KLA	45–61%	3–9%	Book-to-bill + service / installed-base mix	**Export cliff** — a ban can erase 20–40% of the market overnight

THE ONE RULE

Never read a trailing P/E on a commodity cyclical as a bargain. Low P/E at the top, high-or-negative P/E at the bottom — the multiple is backwards exactly when it matters most.

THE ONE SHORTCUT

Match the business model to the risk you're taking. A number that's healthy for a toolmaker can be a warning for a memory maker. Same sector, opposite meaning.

Know what you actually own.

The label on your brokerage app says "semiconductor." This guide says which of six businesses you're really holding — and whether its economics look anything like the story in your head. Fundamentals over narrative, every video.

Watch the full breakdown	YouTube · The Only Semiconductor Stock Guide You'll Ever Need
The interactive margin map	quantrinsiq.com/insights/semiconductor-map
Website	quantrinsiq.com